WAVECREST Corporation

Using *WAVECREST*'s *Virtual Instruments*™ Datacom Software, ver. 3.20, to Evaluate Clock/Transmitter Chip Pairs on Fibre Channel Disk Drive Boards

Application Note No. 129

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WAVECREST Corporation
A Technologies Company
7275 Bush Lake Road
Edina, Minnesota 55439
(612) 831-0030
(800) 733-7128
www.wavecrestcorp.com

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Introduction

One of the most stringent test parameters on a data communications system is transmit jitter. Often, the system performance, compliance and long-term reliability depend on a few picoseconds of difference between jitter performance of the transmitter and the associated reference clock chosen by the system designer. This paper will describe how to set up and interpret the data plots available in *WAVECREST*'s *Virtual Instruments*™ (*VI*), v3.20, DataCom™ software in order to evaluate Fibre Channel Disk Drive controller boards.

Measurement Background

For this experiment, seven types of Fibre Channel disk drive controller boards were available for evaluation. Each of these boards had different reference clocks and different serdes (serial/deserializer) ASICs. Chart 1 outlines the combinations of serdes cells, clocks and crystals used on the evaluation boards.

Chart 1

Clock Vendor	Serdes Vendor
A	1
B	1
C	1
A	2
B	2
C	2
B	3

Both Clock A and Clock B are low-noise PLLs from different clock vendors. Clock C is a crystal oscillator. On the transmitter side, combining the clocks with different vendors' serdes chips can tell us how the clock jitter modulation is affecting the transmitter output jitter. We can now evaluate the ***system*** level performance of the transmit jitter as a function of the clock jitter and the transceiver PLL bandpass characteristics and make qualitative judgements about which chips will provide the best Bit Error performance.

Instrument Setup

An instrument's effectiveness is often tied to the ease of setup when performing certain measurements. In order to evaluate the output stage performance, the setup shown in Figure 1 was used.

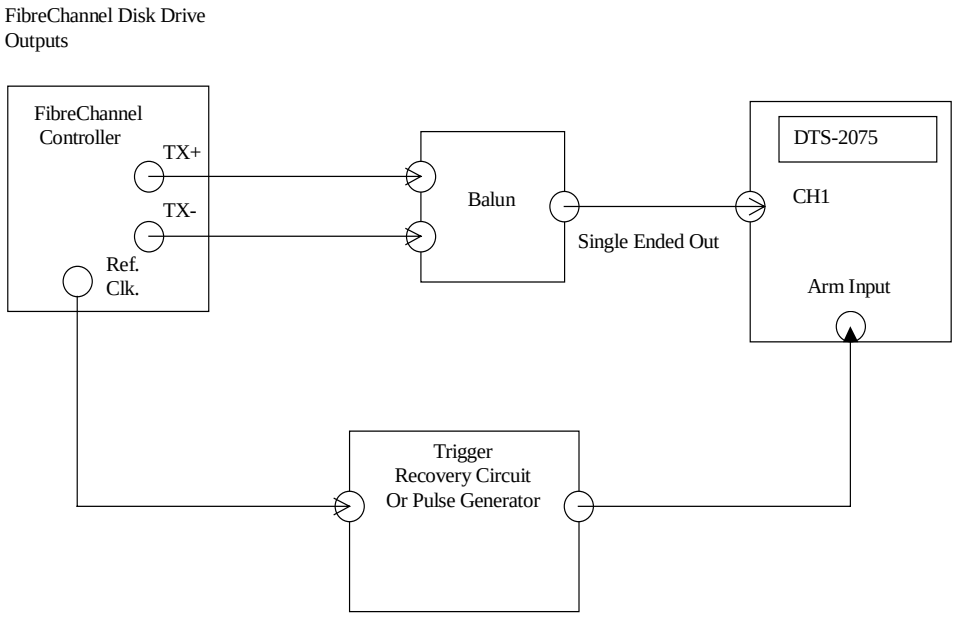


Figure 1 - Instrument Setup

Using an arm signal into the DTS-2075™ (DTS) allows the most accurate, easily correlated measurements of Deterministic Jitter (DJ) and Random Jitter (RJ). Often, a pattern marker is not available on the system board so the arming signal must be recovered from the reference clock. This clock is usually 106.25MHz but may also be 53.125MHz on some boards. Sometimes the 1.0625GHz bit clock is also available from the ASIC. Noteworthy about this setup is that it is flexible enough to obtain the most accurate results since the user can program a known pattern through the Fibre Channel transmitter and use an synchronous arming signal.

Arming the DTS-2075 for Fibre Channel Measurements

The proper trigger for the DTS may be derived from this equation:

Pattern Marker Time = 1.0625GHz / pattern bit length

A 40-bit idle pattern would require an arming signal at 26.0675MHz. A 2^5-1 PRBS pattern would require a 34.274MHz arm frequency. There are two common ways to obtain the arm signal:

1) Use a pulse generator. The Ref Clock is taken off the Fibre Channel board and put into the sync in or PLL input of the pulse generator. The generator is slaved to the reference clock and the generator output is programmed to the proper frequency calculated above.

2) Use a counter or similar circuit that can divide the Ref Clock to the proper arm frequency.

The important thing to achieve with this arming signal is stability. The arm signal must have jitter less then ½ UI (1 Unit Interval = 941ps). If the arm signal has a great deal of jitter, the DTS-2075™ will detect an error in the pattern.

In addition, the arming recovery setup should have the ability to delay the arming signal at least ½ UI. This allows the placement of the arming edge in an unambiguous position. If the arm signal is "on the edge" of the transmit pattern signal, the inherent jitter in the signal might also cause an error. Adding a delay to this signal will fix this error. The relative position of the arm signal inside the pattern is not important, just that it repeats at the same time in the pattern.

Balun

The balun is a passive element which transforms the differential transmit outputs to a single-ended matched impedance signal that the DTS can measure directly. The balun switches at the zero crossing point of the transmit signals. It is important to convert the differential signal to a single-ended signal to maintain the common mode noise rejection and to equalize the differences in the rise and fall times of the output drivers. Differential probes may also be used.

Software Setup

Virtual Instruments™ DataCom is used to measure the total jitter of the transmitter. It is setup as follows:

1) Select DataComm in the Window pull-down menu in the main *VI* control window
2) Select External in the Arming Dialog box under the DTS pull-down menu. This enables the use of an arming signal on the DTS.
3) Under the Options pull-down menu, select Option Dialog.
4) In the dialog box, press the Load from File button. Select the correct pattern that the transmitter is programmed to output. For this experiment we used the Fibre Channel idle pattern. This is called up by selecting `idle.ptn` the directory. The pattern file in ASCII text format is:

```
3eaa2aaaaa
```

The waveform for an idle pattern should look like:

5) Make sure this pattern is correct by observing the waveform displayed in the dialog box.

6) If the pattern does not match, an error message will be displayed when the test is executed. An error may occur because the pattern is not the specified pattern length or the trigger signal is right on a bit transition and the jitter is causing an error. Add some delay to the arming signal and see if the error goes away. If not, try learning the pattern by executing Learn Pattern button.
7) Program the low cutoff frequency. Usually on a Fibre Channel part, this value is set to 637kHz.
8) Click on the OK button and execute the plot by clicking the GO button in the main *VI*™ window.

Measurement Results

The following section contains the FFT plots of the transmit output for the part combinations shown in Chart 1. Figure 2 is the FFT for the first combination in Chart 1.

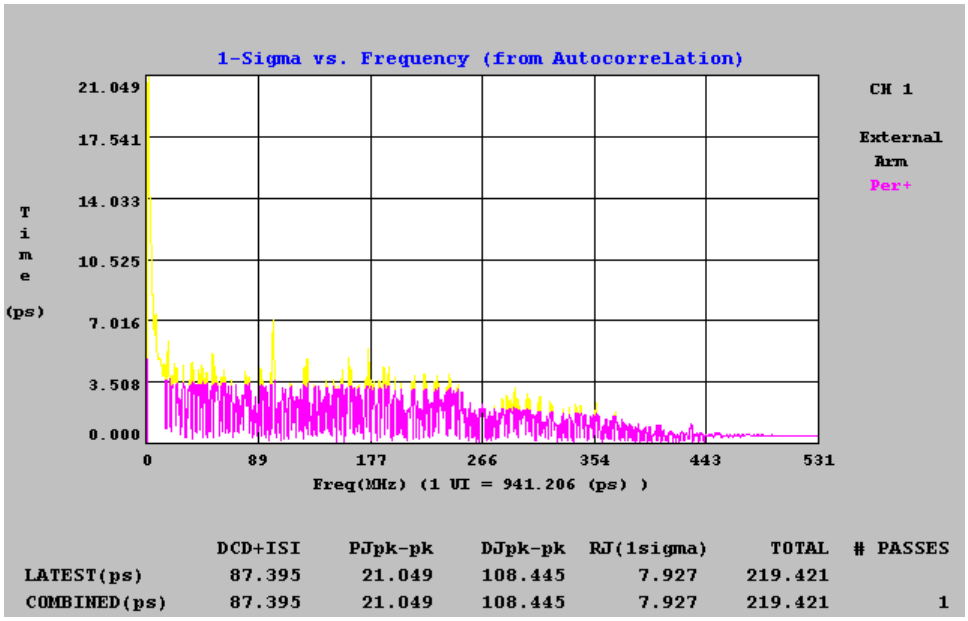


Figure 2 - Clock Vendor A/Serdes Vendor 2

Note the presence of the low frequency periodic spike at 1.2MHz that is contributing 21ps of periodic jitter (PJ pk-pk) This is due to the peaking on the lower end of the transmitter's passband. There is also a spike at 106MHz, most likely a feed-through from the reference clock. The duty cycle distortion is 87.4ps, producing a DJ number of 108ps. The RJ component is 7.9ps. Random Jitter is multiplied by 14 to obtain the Total Jitter (TJ=DJ+14*RJ).

One of the biggest noise contributors is Random Jitter. RJ provides the long-term reliability of the system and may be used to extrapolate BER. Finally, since RJ is multiplied by 14, a 1ps change in RJ is much more significant than a 1 ps change in DJ when viewed as a percentage of total jitter.

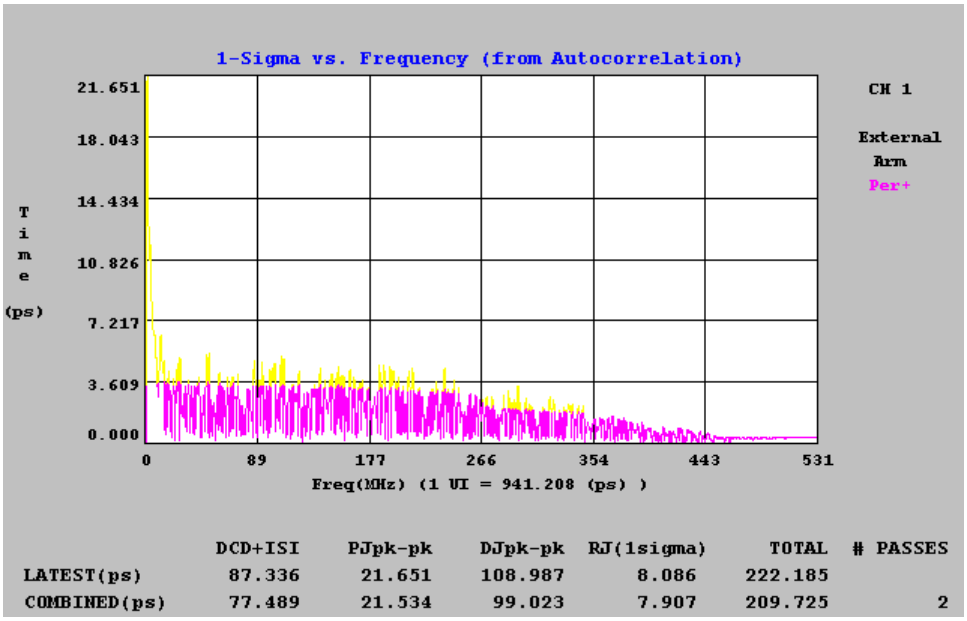


Figure 3 - Clock Vendor B/Serdes Vendor 2

The only difference between Figure 3 and Figure 2 is that a different clock vendor is used. This combination of parts has very similar performance to that of Figure 2, but this clock is producing slightly less high-frequency jitter periodic components. Typically, jitter in the Fibre Channel pass-band tends to degrade system performance so this may be a significant positive for this clock chip. Overall, these two part combinations are performing equally well for both DJ and RJ.

Figures 4 and 5 look at the second serdes vendor with the same two clock chips.

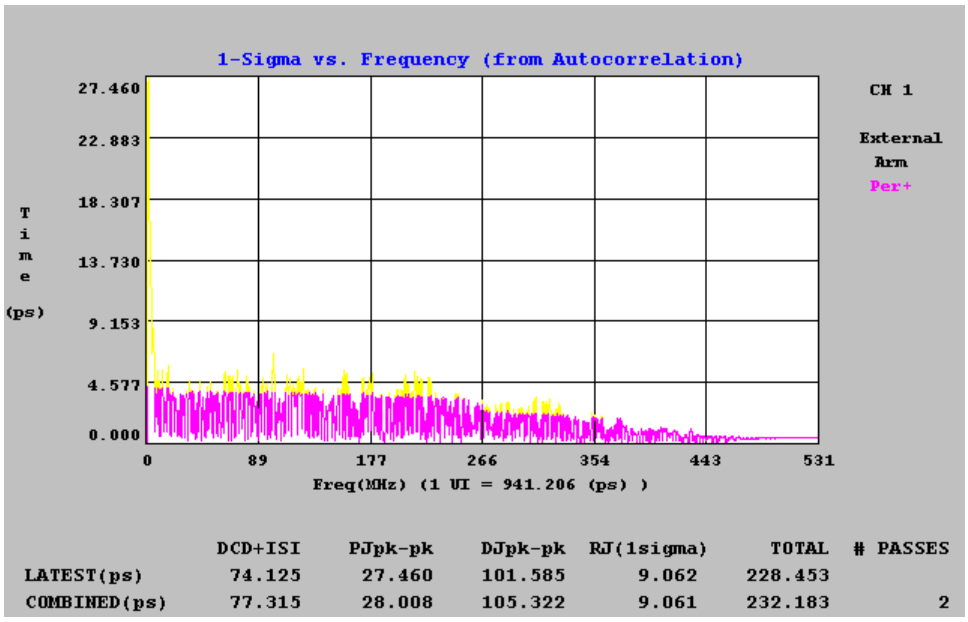
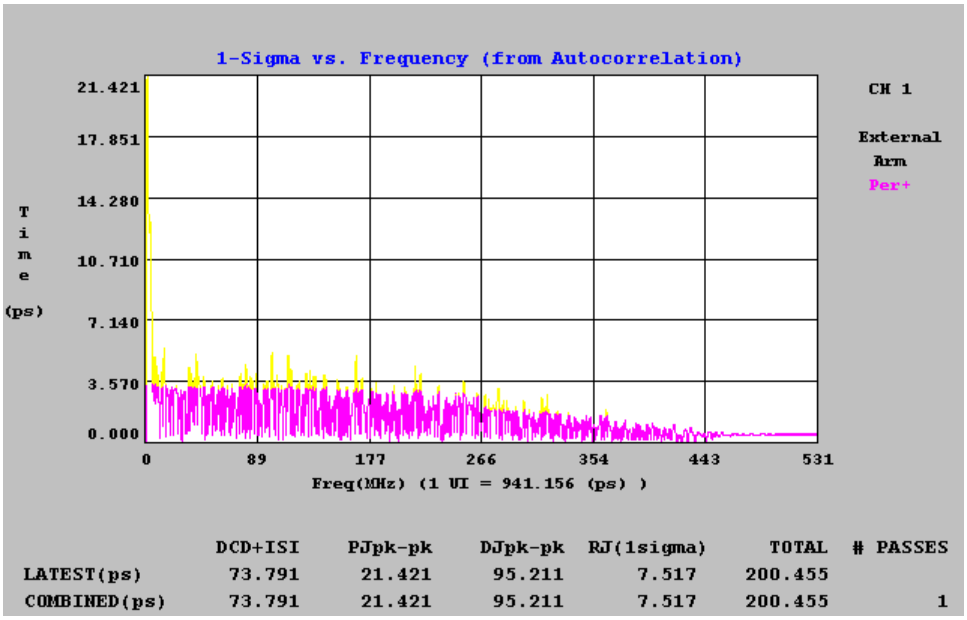


Figure 4 - Serdes Vendor 1/Clock Chip Vendor A

Compare Figure 4 to Figure 2. This part has significantly less DCD/ISI but a larger periodic component of 27ps vs. 21ps. The larger periodic is due to the larger peaking at the 637kHz 3dB point. This part also has a faster PLL loop bandwidth. The smaller DCD+ISI is likely due to the faster rise and fall times of the output stage of this chip. The RJ is larger because more of the peak energy in the FFT is spread through the noise floor of the FFT. This raises the RMS of the noise floor slightly. Also note that the 106MHz period is gone. The ref clock frequency is filtered out by this serdes. The net result is that this combination of parts has a slightly higher TJ because of the 1ps higher RJ. The DCD result may indicate that this serdes might be better in a system with bandwidth constraints.



Picture 5 - Serdes 1/ClockVendor B

Notice the significant improvements in Figure 5. The benefits of the faster outputs on this serdes are seen in the lower DCD numbers from Figure 3. The RJ number is better, most likely as a direct result of a lower periodic spike at 1.2MHz plus the better high-frequency filtering of this part.

Figures 6 and 7 are the same two serdes with a low-noise crystal oscillator. This crystal has very low long-term phase noise and about 7ps of accumulated long-term jitter.

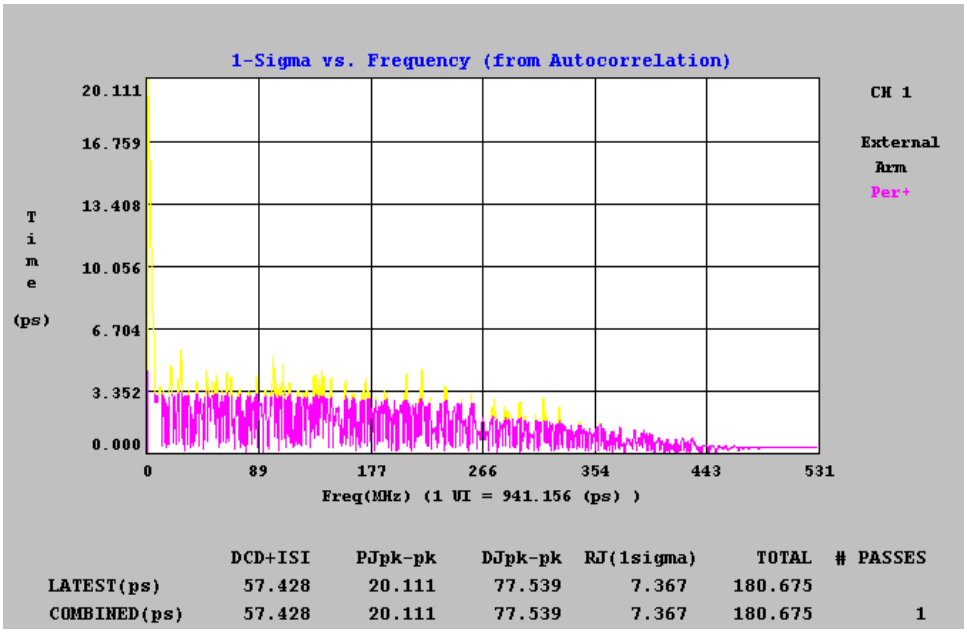


Figure 6 - Crystal Oscillator/Serdes Vendor 1

Note how everything improves. The PJ is lower since the peaking effect of the serdes at the cutoff frequency is amplifying much lower jitter components. The RJ is smaller due to the lower clock noise and the DCD is lower since the edges out of the transmitter are placed more accurately because of the quieter crystal clock.

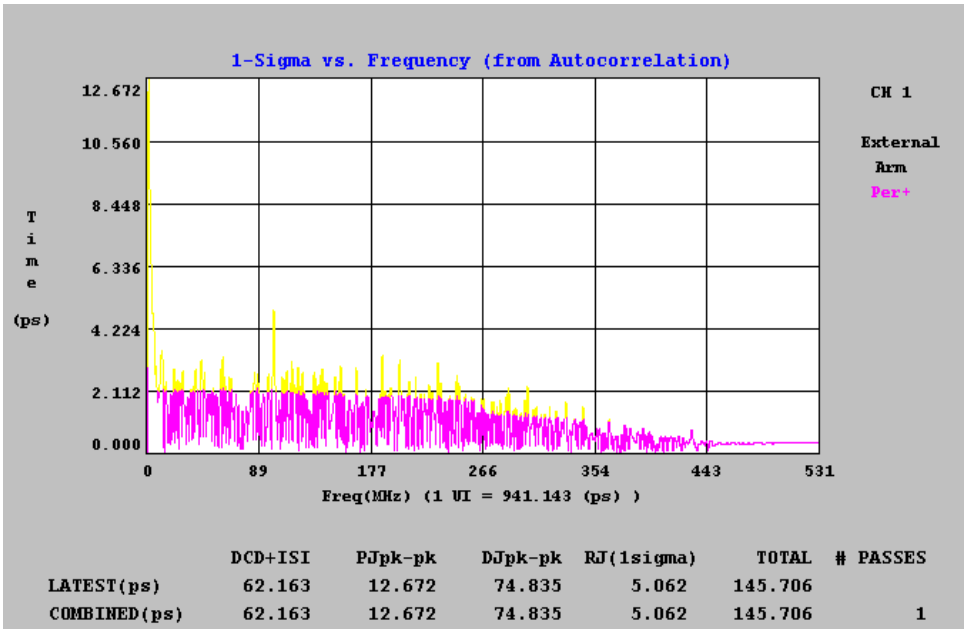


Figure 7 - Serdes Vendor 2 with Crystal Oscillator

The performance of RJ is dramatically improved. Almost 4ps of RJ has been reduced resulting in a 56ps improvement in total jitter. Also, the PJ is about 15ps better and there are improvements in DCD/ISI. The 106MHz clock feed-through is visible because of the lower noise floor. This peak is about 6ps pk-pk.

Finally, Figure 8 is an example of one of the chip combinations with a new board layout and the application of additional filtering.

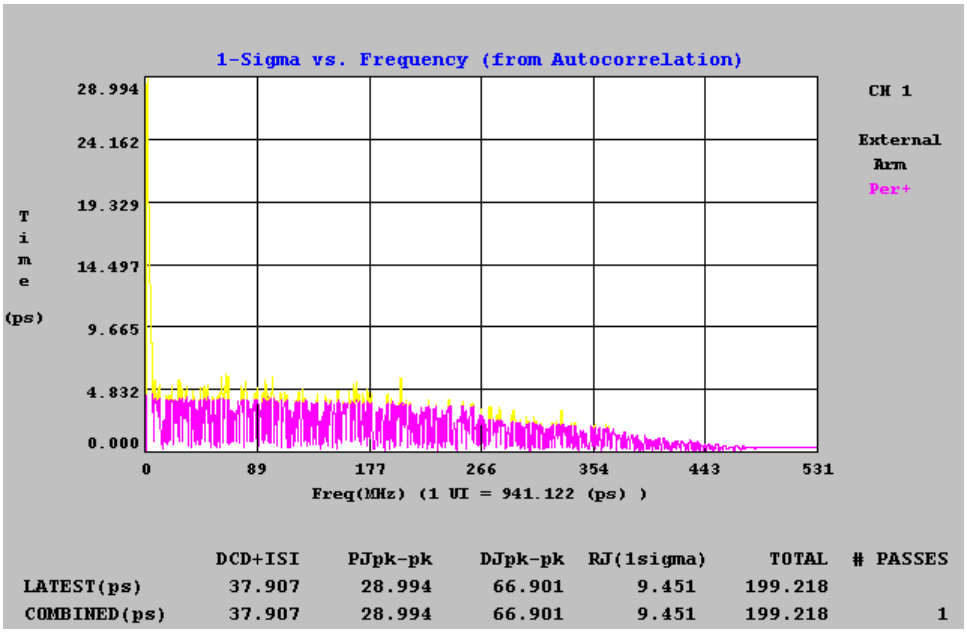


Figure 8 - Serdes Vendor 1/Clock Vendor 1 New Layout

Note how much the DCD/ISI improved by using a better layout. Also, this filter did not change the PJ or RJ numbers.

Data Summary

Chart 2 summarizes the jitter measurements.

Chart 2

Chip Combination	DCD/ISI	PJ	RJ	Total Jitter
Serdes 1/Clock A	77ps	28ps	9.062ps	232.183ps
Serdes1/Clock B	73.79ps	21.42ps	7.517ps	200.455ps
Serdes2/Clock A	87.39ps	21.04ps	7.92ps	219.42ps
Serdes2/Clock B	87.336ps	21.651ps	8.086ps	222.185ps
Serdes1/Xtal Osc.	57.428ps	20.111ps	7.367ps	180.675
Serdes2/Xtal Osc.	62.16ps	12.672ps	5.062ps	145.706ps
Serdes1/Clock1 Improved Layout	37.907ps	28.994ps	9.451ps	199.218ps

Conclusion

The data in Chart 2 shows precisely how to improve this Fibre Channel system. Using the improved layout with Serdes1 and a crystal oscillator produces the best overall performance with an expected total jitter of around 120ps or 0.127UI. In a real system pattern operation, it is expected that this number would get larger as more random data is pushed through the transmitter. The addition of more data will degrade the DCD number, produce more periodic jitter that is often pattern dependent and raise the random noise. These factors will track proportionally through each system so that the relative performance of each should stay constant. The application itself may dictate what cost can be born out to improve jitter performance, but in a datacom application, reliability and bit error rate are the ultimate measures of a product's performance.

WAVECREST's DTS-2075™ and *Virtual Instruments*™ software are ideally suited for this type of analysis. The engineer can characterize datacom applications for all types of jitter. Perhaps even more important, comparison analysis and correlation are accomplished quickly and unambiguously when the user can provide a known pattern and a pattern marker for the *Virtual Instruments*™ software.

Send Comments and Questions about this paper to
Ron Lesnikoski
rlesniko@wavecrestcorp.com

WAVECREST Corporation
World Headquarters
7275 Bush Lake Road
Edina, MN 55439
(612) 831-0030
FAX: (612) 831-4474
Toll Free: 1-800-733-7128
www.wavecrestcorp.com

WAVECREST Corporation
West Coast Office:
1735 Technology Drive, Suite 400
San Jose, CA 95110
(408) 436-9000
FAX: (408) 436-9001
1-800-821-2272